The Claims Patentably Define the Invention Over Breternitz

The Examiner rejected claims 1-10 primarily over Breternitz Jr. et al. (U.S. Patent No. 6,216,213, hereinafter referred to as the "Breternitz patent"). Claims 1-5 and 7-10 were rejected under 35 U.S.C. § 102(e) solely due to the Breternitz patent; claim 6 was rejected under 35 U.S.C. § 103(a) over the Breternitz patent in view of an article entitled "Low Entropy Image Pyramids for Efficient Lossless Coding."

A claim is anticipated under Section 102 only "if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987); MPEP 2131. "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236 (Fed. Cir. 1989).

The Breternitz patent is directed to compression of "instruction memory for use in a cache system." Col. 2, lines 41-45. As described in detail in the specification, the Breternitz patent describes a method of speeding up the work of a microprocessor cache by simplifying address translation of compressed cache line blocks. See Col. 2, lines 1-13, 41-67. As is well known in the microprocessor hardware cache art, a "cache line" or "cache block" is a unit of memory that can be transferred between the main memory and the cache. See, e.g., "The Free Online Dictionary of Computing," http://burks.brighton.ac.uk/burks/foldoc/17/16.htm. It is well-known in fabricating modern microprocessors to include hardware caching technology to speed up execution of processor instructions. Apparently, before the Breternitz patent, prior art microprocessor architectures required translation of an address tag into a compressed address location to identify the location of a particular block of compressed memory instructions. See Col. 2, lines 1-13. The Breternitz patent simplifies this address translation process by providing a "one-to-one correlation between the address tag and the compressed memory." See Col. 2, lines 53-67.

As noted by the Examiner, each claim of the present invention includes as a limitation the transformation of data "in accordance with a schema" or, in the case of claim 6, the generation of a "schema for improving compression of a stream of data". The Examiner argues in the outstanding Office Action that this claim limitation is reflected in the following passage from the Breternitz patent:

> After compression and upon subsequent decompression, this transformed address is to be quickly and unambiguously divisible into the starting address of the compressed cache line in

> compressed memory and the word offset identifying the instruction location within the cache line.

Col. 3, lines 24-29.

The Examiner's rejection appears to reflect some confusion regarding what is being "transformed" as well as the terms "schema" (as utilized in the present application) and "cache line block" (as utilized in the Breternitz patent). The cache line, as alluded to above, represents a data channel between main memory and a hardware cache for a microprocessor that is limited to blocks of data referred to as a "cache line block" in the Breternitz patent. Each processor instruction in the cache line has an address in the cache memory. The address represents a way of locating the data in the cache memory. Because of the above-described "one-to-one correlation" between address tag and compressed memory address, the Breternitz patent permits the microprocessor architecture to quickly locate the cache processor instructions. What is being translated/"transformed" is not the compressed processor instructions, but the *address* of the processor instructions.

In contrast, the present invention has nothing to do with optimizing memory access to a processor cache of processor instructions. At a very minimum, it can be said that it is the data itself that is being transformed "in accordance with a schema" – not a memory address to the data.

Moreover, the fact that in the Breternitz patent, the "memory (20) is divided into cache line blocks (500)" (Abstract) has nothing to do with the schema transformation process described in the present invention. In the Breternitz patent, the memory is divided into blocks that fit the hardware limitation of the channel existing between the main memory and the cache memory. This is a hardware specification that is processor-dependent. The division into cache line blocks reflects no "transformation in accordance with a schema" as that would be understood by one of ordinary skill in the art with reference to the present specification. In fact, the stream of data processor instructions itself is not "transformed" at all prior to compression; nor is it ever referred to in the Breternitz patent as being "transformed" prior to compression.

Applicants respectfully submit that the claims in their original form represent allowable subject matter. Accordingly, a Notice of Allowance to this effect is earnestly solicited.

The Examiner is invited to contact the undersigned at 908-221-5438 to discuss any matter concerning the application.

The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C. F. R. 1.16 and 1.17 to **AT&T Corp. Deposit Account No. 01-2745 .**

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